UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,534	11/26/2003	Dean A. Klein	MTIPAT.024DV4	1855

20995 7590 11/18/2005

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
LEE, CHUN KUAN	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,534	KLEIN, DEAN A.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/26/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 48 is objected to because of the following informalities:

In claim 48, line 1, "The cache memory circuit of Claim 43" should be changed to -- The cache memory circuit of Claim 41 --. Correction is required.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 4, 12, 14-16, 21, 23, 29, 31, 36 and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Ireton (US Patent 6,711,667).

3. As per claim 1, Ireton teaches a system method including searching function for cache memory management comprising:

receiving an instruction to perform a search operation, the instruction comprising a fetch address for the search operation (Figures 1-2 and column 6, lines 5-51, where "fetch address" is read on "starting address");

routing the instruction to a instruction fetch control (Figures 1-2, where "instruction fetch control" is read on "data string manipulation circuit");

routing the fetch address for the search operation from the instruction fetch control to a cache storage and control block and a storage control unit (Figures 1-3,

column 6, lines 5-51 and column 8, lines 12-67, where "cache storage and control block and storage control unit" is read on "cache memory array");

comparing the fetch address to the addresses stored in the storage control unit (Figures 1-3 and column 7, line 52 to column 8, line 67, where "fetch address " is read on "test data string", "addresses" is read on "data" and "storage control unit " is read on "cache memory array"); and

routing a instruction of the of cached data matching the fetch address to a instructor decode unit (Figures 1-3 and column 8, lines 12-67, where "instruction" is read on "address" and "instructor decode unit" is read on "data string manipulation circuit").

4. As per claim 2, Ireton teaches the system method including searching function for cache memory management comprising routing the fetch address from the instruction fetch control to the storage control unit (Figures 1-3, column 6, lines 5-23 and column 8, lines 12-67).

5. As per claim 4, Ireton teaches the system method including searching function for cache memory management comprising wherein said act of routing a corresponding address of cached addresses is performed by a plurality of multiplexor circuits, (Figure 2 and column 7, lines 1-8, where "plurality of multiplexor circuits" is read on "decoder").

6. As per claim 12, Ireton teaches the system method including searching function for cache memory management comprising:

receiving an instruction to perform a search operation, the instruction comprising a fetch address and an address of the original code sequence (Figures 1-3, column 6, lines 5-51 and column 7, lines 24-34, where "fetch address" is read on "starting address" and "address of the original code sequence" is read on "test data string");

routing the instruction to a instruction fetch control (Figures 1-2);

routing the fetch address for the search operation from the instruction fetch control to a cache storage and control block and a storage control unit (Figures 1-3, column 6, lines 5-51 and column 8, lines 12-67);

searching a cache line in the cache memory for data that matches the address of the original code sequence, wherein said cache line comprises more bytes than the address of the original code sequence (Figures 1-3, column 5, lines 3-23, column 7, lines 24-34 and column 7, line 52 to column 8, line 67)

routing an instruction of cached data matching the address of the original code sequence to the instruction decode unit (Figures 1-3 and column 8, lines 12-67, where "instruction decode unit " is read on "data string manipulation circuit").

7. As per claim 14, Ireton teaches the system method including searching function for cache memory management comprising wherein the data string manipulation circuit comprises a bus interface unit (Ref # 22 in Figure 1).

8. As per claim 15, Ireton teaches the system method including searching function for cache memory management comprising wherein the data string manipulation circuit comprises a controller (Ref # 54 in Figure 3, where "controller" is read on "memory controller").

9. As per claim 16, Ireton teaches the system method including searching function for cache memory management comprising wherein said act of routing a corresponding address of cached addresses is performed by a plurality of multiplexor circuits, (Figure 2 and column 7, lines 1-8).

10. As per claim 21, Ireton teaches the system method including searching function for cache memory management comprising wherein said act of routing an address of the matching cached data comprises routing the address of the matching cached data with stored in the storage control unit if there are a plurality of matches in the cache line (column 7, line 52 to column 8, line 67, where "stored in the storage control unit" is read on "lowest address").

11. As per claim 23, Ireton teaches the system method including searching function for cache memory management comprising:

a storage control unit comprising a cache line comprising a plurality of bytes of data (Figures 3-5, column 5, lines 3-23 and column 7, lines 24-34, where "storage control unit" is read on "cache data memory");

an instruction fetch control block configured to form a fetch address, the fetch address comprising less bytes than the cache line (Figures 2-3, column 6, lines 5-24 and column 7, lines 24-34, where "instruction fetch control block" is read on "data source" and "fetch address" is read on "data value");

a cache storage and control block and the storage control unit configured to search the entire cache line for data matching the fetch address, comprising (Figures 1-3, column 6, lines 5-51 and column 7, line 24 to column 8 line 67, where "cache storage and control block and storage control unit" is read on "instruction processor"):

a first set of inputs coupled to the tag storage, each of the first set of inputs configured to receive at least one of said plurality of bytes of data of the cache line (Ref # 54 and 56 in Figure 3, where "tag storage" is read on "cache data storage");

a second set of inputs coupled to the fetch address and configured to receive at least a portion of the data value from the fetch data (Ref # 36 in Figure 3); and

a plurality of outputs (Figure 2); and

a plurality of multiplexor circuits coupled to the outputs of the cache storage and control block and the storage control unit and configured to identify a portion of the cache line that matches at least a portion of the fetch address (Figure 2, column 7, lines 1-31, where "plurality of multiplexor circuits" is read on "decoder").

12. As per claim 29, Ireton teaches the system method including searching function for cache memory management comprising wherein the fetch address comprises a plurality of bytes (column 5, lines 3-23, where "fetch address" is read on "data value").

13. As per claim 31, Ireton teaches the system method including searching function for cache memory management comprising:

a storage control unit comprising a plurality of cache lines, each cache line comprising a plurality of bytes of data (Figure 3, column 5, lines 3-23 and column 7, line 52 to column 8, line 11, where "storage control unit" is read on "data memory");

an instruction cache block configured to receive an address of the original code sequence and an instruction to perform a search operation, the instruction processing circuit comprising a plurality of inputs coupled to the storage control unit such that each input is coupled to receive one of the plurality of bytes of data of the cache line, the instruction cache block further comprising a plurality of outputs (Figures 1-3, column 7, lines 24-34 and column 7, line 52 to column 8, line 49, where "instruction cache block" is read on "instruction processing circuit" and "address of the original code sequence" is read on "test data string"); and

a plurality of multiplexor circuits coupled to the plurality of outputs of the instruction cache block and configured to identify a portion of the cache line having data that matches at least a portion of the address of the original code sequence (Figure 2, column 6, line 52 to column 7, line 32, where "plurality of multiplexor circuits" is read on "decoder").

14. As per claim 36, Ireton as modified teaches the system method including searching function for cache memory management comprising wherein the address of the original code sequence comprises a plurality of bytes (column 5, lines 3-23).

15. As per claim 39, Ireton teaches the system method including searching function for cache memory management comprising wherein the instruction cache block further comprises a controller (Ref # 54 in Figure 3, where "controller" is read on "memory controller").

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 3, 8-9, 13, 18, 19, 24-26 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ireton (US Patent 6,711,667) as applied to claims 1, 12, 23 and 31 above, and further in view of Wan (US Patent 5,710,905).

17. As per claim 3, Ireton does not teach the system method including searching function for cache memory management comprising aligning the fetch address with the addresses stored in the storage control unit prior to said act of comparing.

Wan teaches a system method for cache memory management comprising aligning an address from the host processor bus with the addresses stored in the cache tag memory prior to said act of comparing (Figure 2 and column 4, lines 38-53, where "address from the host processor bus" is read on "test data string" and "cache tag memory" is read on "cache memory array").

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Ireton to include aligning the address from the host processor with the addresses stored in the cache tag memory prior to said act of comparing.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modified Ireton by the teaching of Wan, because including aligning the address from the host processor with the addresses stored in the cache tag memory prior to said act of comparing, would enable the cache controller of the cache memory management system method to further support "non-symmetric" caches.

18. As per claim 8, Ireton as modified teaches the system method including searching function for cache memory management comprising wherein said act of comparing is performed by a plurality of comparators (Wan, Figure 2).

19. As per claim 9, Ireton as modified teaches the system method including searching function for cache memory management comprising wherein the number of the plurality of comparators is equal to the number of addresses in the cache tag

memory (Ireton, column 5, lines 3-23 and Wan, Figure 2, where "addresses" is read on "number of bytes in a cache line").

20. Claims 13 and 18-19 repeat the limitations of claims 3 and 8-9 and are therefore rejected accordingly.

21. As per claim 24, Ireton does not teach the system method including searching function for cache memory management comprising wherein the instruction processor comprises a plurality of comparators.

Wan teaches a system method for cache memory management comprising wherein the cache controller comprises a plurality of comparators. (Figure 2, where "cache controller" is read on "instruction processor").

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to combine Ireton and Wan for reason stated above.

22. As per claim 25, Ireton as modified teaches the system method including searching function for cache memory management comprising wherein each comparator is coupled to one input of the first set of inputs, one input of the second set of inputs, and one output (Wan, Figure 2).

23. As per claim 26, Ireton as modified teaches the system method including searching function for cache memory management comprising wherein the plurality of

multiplexers are configured to identify the matching portions of the cache line when matches from the cache storage and control block and the storage control unit are detected (Ireton, Figure 2, column 6, line 52 to column 7, line 23 and column 8, lines 12-26, where "cache storage and control block and the storage control unit" is read on "at least two of the comparators").

24. Claims 32-34 repeat the limitations of claims 24-26 and are therefore rejected accordingly.

25. Claims 5-7 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ireton (US Patent 6,711,667) as applied to claims 1 and 12 above, and further in view of Sachs et al. (US Patent 4,860,192).

26. As per claims 5-7, Ireton does not teach the system method including searching function for cache memory management comprising wherein the fetch address comprises a word;

wherein the fetch address comprises a doubleword; and

wherein the fetch address comprises a quadword.

Sachs teaches a cache system method wherein the cache memory stores a singleword per addressable line of cache storage (column 7, lines 1-5, where "singleword" is read on "word");

wherein the cache memory stores a doubleword per addressable line of cache storage (column 7, lines 1-5); and

wherein the cache memory stores a quadword per addressable line of cache storage (column 2, lines 26-34).

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modified Ireton to include the system method for cache memory management comprising wherein the fetch address comprises a singleword;

wherein the fetch address comprises a doubleword; and

wherein the fetch address comprises a quadword.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modify Ireton by the teaching of Sachs, because including the system method for cache memory management comprising wherein the fetch address comprises a singleword;

wherein the fetch address comprises a doubleword; and

wherein the fetch address comprises a quadword,

would allow the system method including searching function for cache memory management to incorporate multiple-word cache memory management.

27. Claim 22 repeats the limitations of claims 5 and is therefore rejected accordingly.

28. Claims 10-11, 17, 20, 30, 35, 37, 40-46 and 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ireton (US Patent 6,711,667) as applied to claims 1, 12, 23 and 31 above, and further in view of Tran et al. (US Patent 5,764,946).

29. As per claims 10-11, Ireton teaches the system method including searching function for cache memory management comprising the prefetch functionality (Figure 2, Figure 6 and column 10, lines 7-37)

Ireton does not teach the system method including searching function for cache memory management comprising wherein said act of comparing is performed with a plurality of subtractors and said act of comparing is performed in one clock cycle.

Tran teaches the system method for predicting an instruction fetch within an Instruction cache comprising:

wherein said act of fetching address is performed with a plurality of subtractors (column 37, lines 7-20 and column 38, line 24-33, where "fetching address" is read on "comparing"); and

wherein said act of comparing is performed in one clock cycle (Figure 4B).

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Ireton to include the system method for cache memory management comprising:

wherein said act of fetching address is performed with a plurality of subtractors; and

wherein said act of comparing is performed in one clock cycle.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modified Ireton by the teaching of Tran, because including the system method for cache memory management comprising:

wherein said act of fetching address is performed with a plurality of subtractors; and

wherein said act of comparing is performed in one clock cycle, would achieve overall better performance.

30. Claims 17and 20 repeat the limitations of claims 10-11 and are therefore rejected accordingly.

31. Claim 30 repeat the limitations of claim 11 and is therefore rejected accordingly.

32. Claims 35 and 37 repeat the limitations of claims 10-11 and are therefore rejected accordingly.

33. As per claim 40, Ireton as modified teaches the system method including searching function for cache memory management comprising:

A data source means for providing a fetch address (Figure 2 and column 6, lines 5-24, where "providing" is read on "holding" and "fetch address" is read on "data value");

a cache data memory means for holding at least one cache line comprising a plurality of bytes of data (Figure 3, column 7, lines 24-32); and

a means for searching the cache line, wherein said means for searching is coupled to said cache data memory means and said data source means (Figures 2-3 and column 6, line 5 to column 8, line 67).

Ireton does not teach the system method including searching function for cache memory management comprising wherein said means for searching is performed in one clock cycle for data that matches the fetch address.

Tran teaches the system method for predicting an instruction fetch within an Instruction cache comprising: wherein said act of comparing is performed in one clock cycle (Figure 4B).

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to combine Ireton and Tran for reason stated above.

34. As per claim 41, Ireton as modified teaches the system method including searching function for cache memory management comprising a plurality of multiplexers coupled to the means for searching, wherein the plurality of multiplexers identifies a portion of the cache line that matches at least a portion of the fetch address (Ireton, Figure 2, column 6, line 52 to column 7, line 32 "plurality of multiplexers" is read on "means for decoding").

35. As per claim 42, Ireton as modified teaches the system method including searching function for cache memory management comprising wherein the means for

searching comprises a plurality of subtractors (Tran, column 37, lines 7-20 and column 38, lines 24-33).

36. As per claim 43, Ireton as modified teaches the system method including searching function for cache memory management comprising wherein the means for searching comprises a plurality of comparators (Tran, column 53, line 42 to column 54, line 40).

37. As per claim 44, Ireton as modified teaches the system method including searching function for cache memory management comprising wherein the number of comparators is equal to the number of bytes of address in the cache line (Tran, column 53, line 42 to column 54, line 40).

38. As per claim 45, Ireton as modified teaches the system method including searching function for cache memory management comprising wherein the data source means comprises an instruction fetch control block and a bus interface unit (Ireton, Ref # 22 in Figure 1 and Ref # 30 in Figure 2, where "instruction fetch control block and bus interface unit" is read on "external string execution circuit").

39. As per claim 46, Ireton as modified teaches the system method including searching function for cache memory management comprising wherein the external string execution circuit comprises the bus interface unit (Ireton, Ref # 22 in Figure 1).

40. As per claim 48, Ireton as modified teaches the system method including searching function for cache memory management comprising wherein the plurality of multiplexers are configured to identify the matching portions of the cache line when matches from the cache storage and control block and the storage control unit are detected (Ireton, Figure 2, column 6, line 52 to column 7, line 23 and column 8, lines 12-26, where "cache storage and control block and the storage control unit" is read on "at least two of the comparators").

41. As per claim 49, Ireton as modified teaches the system method including searching function for cache memory management comprising wherein the fetch address comprises a plurality of bytes (Ireton, column 5, lines 3-23).

42. Claims 27-28 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ireton (US Patent 6,711,667) as applied to claims 23 and 31 above, and further in view of Hicks et al. (US Patent 6,085,291).

43. As per claim 27, Ireton teaches the system method including searching function for cache memory management comprising the prefetch functionality (Figure 2, Figure 6 and column 10, lines 7-37).

Ireton does not teach that the system method including searching function for cache memory management comprising wherein the cache data memory comprises a Level 1 cache.

Hicks teaches the system method for cache memory management comprising wherein the cache data memory comprises a L1 cache (Figure 1, column 2, lines 28-38 and column 3, line 56 to column 4, line 15, where "L1" is read on "Level 1").

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Ireton to include the system method for cache memory management comprising wherein the cache data memory comprises a L1 cache.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modified Ireton by the teaching of Hicks, because including the system method for cache memory management comprising wherein the cache data memory comprises a L1 cache, would enable the reduction in latency of data and instruction accesses to L1 cache without lowering the performance of microprocessor.

44. As per claim 28, Ireton as modified teaches the system method for cache memory management comprising wherein the cache data memory comprises a L2 cache (Figure 1, column 2, lines 28-38 and column 3, line 56 to column 4, line 15, where "L2" is read on "Level 2").

45. Claim 38 repeat the limitations of claim 27 and is therefore rejected accordingly.

46. Claim 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ireton (US Patent 6,711,667) and Tran et al. (US Patent 5,764,946) as applied to claim 45 above, and further in view of Hicks et al. (US Patent 6,085,291).

47. As per claim 47, Ireton teaches the system method for cache memory management comprising the prefetch functionality (Figure 2, Figure 6 and column 10, lines 7-37) and the external string execution circuit comprising of the bus interface unit is coupled to the system bus (Ref # 22 in Figure 1).

Ireton does not teach that the system method for cache memory management comprising wherein the external string execution circuit is associated with an off-chip memory controller.

Hicks teaches the system method for cache memory management comprising wherein the system bus is coupled with an off-chip memory controller (Ref # 104 and 124 in Figure 1 and column 3, lines 56-66).

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Ireton as modified to include the system method for cache memory management comprising the external string execution circuit is associated with an off-chip memory controller.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modified Ireton as modified by the teaching of Hicks, because it is well know in the art for the coupling of the system bus interface to be

couple to an off-chip memory controller related to the utilization of prefetching, thus enabling the reduction in latency of data and instruction accesses without lowering the performance of microprocessor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671 and email is chun-kuan.lee@uspto.gov. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Popovici Dov can be reached on (571)272-4083. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Mailed responses to this action should be sent to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231.

Faxes for Official/formal (After Final) communications or for informal or draft communications (please label "PROPOSED" or "DRAFT") sent to:

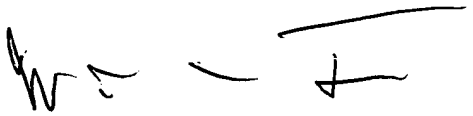
(571) 273-8300

Hand-delivered responses should be brought to:

USTPO, Randolph Building, Customer Service Window

401 Dulany Street

Alexandria, VA 22314



C.K.L.
11/01/2005

WILLIAM M. TREAT
PRIMARY EXAMINER